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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

NO FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision,
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.
See 37 C.F.R. §§ 1.27 AND 1.28

	Complete if Known
Application Number	10/029,547
Filing Date	December 21, 2001
First Named Inventor	ALOK JAIN
Examiner Name	HUGH M. JONES
Group/Art Unit	2128
Attorney Docket No.	15448-0505

TOTAL AMOUNT OF PAYMENT	($) 0.00

METHOD OF PAYMENT (check one)

1. ☒ Throughout the pendency of this application, please charge any additional fees, including any required extension of time fees, and credit all overpayments to deposit account 50-1302. A duplicate of this sheet is enclosed.

Deposit Account Number: 50-1302

Deposit Account Name: Hickman Palermo Truong & Becker, LLP

2. ☐ Payment Enclosed:
☐ Check ☐ Money Order ☐ Other

3. ☐ Applicant(s) is entitled to small entity status. See 37 CFR 1.27.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1011	300	2011	150	Utility filing fee	
1111	500	2111	250	Utility Search fee	
1311	200	2311	100	Utility Examination fee	
1081	250	2081	125	Utility Application Size Fee	
1005	200	2005	100	Provisional Application Fee	
1085	250	20835	125	Provisional Application Size Fee	
				SUBTOTAL (1)	($) 0.00

2. EXTRA CLAIM FEES

	Highest Paid Claims		Extra Claims		Fee from Below		Fee Paid
Total Claims	39	-39 =	0	X	50.00	=	0.00
Independent Claims	3	- 3 =	0	X	200.00	=	0.00
Multiple Dependent						=	

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple dependent claim, if not paid
1204	200	2204	100	**Reissue independent claims over original patent
1205	50	2205	25	**Reissue claims in excess of 20 and over original patent
				SUBTOTAL (2) ($) 0.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge – late filing fee or oath	
1052	50	2052	25	Surcharge – late provisional filing fee or cover sheet.	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1452	500	2452	250	Petition to revive – unavoidable	
1453	1,500	2453	750	Petition to revive – unintentional	
1501	1,400	2501	700	Utility issue fee (or reissue)	
1502	800	2502	400	Design issue fee	
1504	300	2504	300	Publication Fee	
1462	400	1462	400	Petitions Director not specifically provided for Group I	
1463	200	1463	200	Petitions Director not specifically provided for Group II	
1464	130	1464	130	Petitions Director not specifically provided for Group III	
1806	180	1806	180	Submission of information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
				Other fee (specify)	
				Other fee (specify)	

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 0.00

SUBMITTED BY

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Signature				Date	October 26, 2005

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Docket No.: 15448-0505

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Alok Jain, et al.

Serial No.: 10/029,547

Filed: December 21, 2001

For: MECHANISM FOR RECOGNIZING AND ABSTRACTING MEMORY STRUCTURES

Confirmation No.: 4676

Group Art Unit No.: 2128

Examiner: Hugh M. Jones

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

RESPONSE PURSUANT TO 37 C.F.R. § 1.111

Sir:

This is in response to the Office Action mailed August 10, 2005, the shortened statutory period for which runs until November 10, 2005. This response is presented in the format allowed by the Notice of the Office of Patent Legal Administration issued January 31, 2003.

There are no amendments to the specification or the claims. Remarks are presented on separate sheets below.

REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested. No claims have been amended, canceled, or added. Claims 1-39 are currently pending in the application.

CLAIM REJECTIONS – 35 U.S.C. § 103

In the Office Action, the Examiner rejected Claims 1-39 under 35 U.S.C. § 103(a) as being unpatentable over Kramer, U.S. Pat. No. 6,044,004 in view of Allred, U.S. Pat. No. 5,734,798. The rejection is respectfully traversed.

Independent Claim 1

> 1. A computer implemented method for functionally abstracting a memory column, comprising:
> identifying, in a description of a circuit, at least one column of n memory cells, where n is an integer greater than 1;
> representing said column of n memory cells as a single-memory-cell column comprising a single representative memory cell;
> abstracting at least a portion of said single-memory-cell column to derive a logic-level representation for said representative memory cell; and
> generating one or more additional instances of said logic-level representation to derive an abstracted memory column comprising a plurality of instances of said logic-level representation. (Emphasis added)

The method of Claim 1 provides an advantageous way to functionally abstract a memory column. According to Claim 1, this is achieved by identifying at least one column comprising a plurality of memory cells. Once a column of memory cells is identified, a single representative memory cell is chosen and the column of memory cells is represented as a single-memory-cell column comprising the representative memory cell. Next, at least a portion of the single-memory cell column is abstracted to derive a logic-level representation of the representative memory cell. Finally, additional instances of the logic-level representation of the memory cell are generated to derive the full memory

column. By doing so, the full memory column has been abstracted into the logic level without compromising the functionality of the memory column on the logic level. Thus, the method of Claim 1 provides a method for abstracting a memory column which accurately captures the functionality of the overall memory column on the logic level.

Such a method is not disclosed or suggested by Kramer taken individually. Instead, Kramer teaches a floating gate memory device for storing both analog and digital data. Specifically, the memory device includes an array of floating gate FET memory cells divided into sectors. Each sector includes one or more groups of floating gate FET memory cells having sources coupled to a common row line of the memory array.

Several points should be noted about Kramer. First, note that unlike Claim 1, Kramer does not teach or suggest generating one or more additional instances of a logic level representation for a representative memory cell to derive an abstracted memory column. Kramer is completely lacking in any language suggesting the abstraction of a memory column. In fact, in the Office Action, the Examiner noted that Kramer fails to disclose any functional abstraction of the memory array. Therefore, Kramer fails to disclose this aspect of Claim 1.

Next, it should be noted that Kramer does not teach or suggest representing a column of memory cells as a single-memory cell column comprising a representative memory cell. Instead, in Kramer, an array of memory cells is divided into sectors, and each sector includes one or more groups of memory cells having sources coupled to a common row line of the array. However, nothing in Kramer indicates that one such memory cell may be representative of a column of memory cells in a single-memory cell column. Even assuming a "group of memory cells" is equivalent to the column of memory cells in Claim 1, there is no indication that any one memory cell may be

representative of any of the groups of memory cells. In contrast, the method of Claim 1 allows a column of memory cells to be represented by a representative memory cell during the abstraction process. Thus, Applicant respectfully submits that this aspect of Claim 1 is not disclosed or suggested by Kramer.

Therefore, because Kramer does not disclose or suggest the method of Claim 1, Claim 1 is patentable over Kramer, taken individually.

The same is also true for Allred. The method of Claim 1 is not disclosed or suggested by Allred, taken individually. Instead, Allred discloses abstracting a gate modeled circuit from a FET (field effect transistor) modeled circuit utilizing a structurally based Boolean tree. To advance this process, Allred teaches recognizing and removing redundant FETs and FET structures. Redundant parallel FETs are FETs that share common source, drain and gate connections. Additionally, removal of FET structures requires 1) that all FET gate signals in a tree of one FET structure be identical to the corresponding FET gate signals in a redundant FET structure and 2) that a FET structure does not include a feedback loop. Thus, Allred teaches declaring particular FET instances to be redundant and forces their removal from the Boolean tree.

Several points should be noted about Allred. First, note that, unlike Claim 1, Allred does not generate one or more additional instances of a logic level representation for a representative memory cell to derive an abstracted memory column. Rather, the abstraction method disclosed in Allred merely describes removing redundant FETs and FET structures. Allred thus implies *permanently* removing the redundant FET and FET structures. The abstraction method in Allred is not interested in re-creating the redundant FET or FET structures after the abstraction has occurred. In contrast, Claim 1 provides a novel method by generating the additional instances of the logic level representation of a

representative memory cell to derive an abstracted memory column. Thus, the abstracted memory column accurately captures the functionality of the transistor-level memory column.

In support of the contention that this element of Claim 1 is disclosed in Allred, the Examiner points to several excerpts in which removal of redundant FETs is discussed. In none of these excerpts, however, is it disclosed or suggested that Allred generates one or more instances of a logic level representation for a representative memory cell to derive an abstracted memory column. As far as Applicants can see, this aspect of Claim 1 is completely absent from Allred.

Next, note that unlike Claim 1, Allred does not teach representing a column of memory cells as a single-memory cell column comprising a representative memory cell. Rather, as indicated above, Allred teaches removing redundant FETs such that if two or more FETs share common source, drain and gate connections, all but one of them can be removed. However, Allred is devoid of any language suggesting that the remaining FET is actually representative of the removed FETs. The "removal" of redundant FETs is not indicative of "representing" those FETs with the remaining FET. To the contrary, Allred implies the removed FETs are simply left out of the abstraction process. There is no "representation" of removed FETs in Allred. Quite differently, the method of Claim 1 allows a column of memory cells to be represented as a single-memory cell column thus keeping the column itself intact and in place during the abstraction. Consequently, Applicants respectfully submit that this aspect of Claim 1 is not disclosed or suggested by Allred.

Therefore, because Allred does not disclose or suggest the method of Claim 1, Claim 1 is patentable over Allred, taken inidividually.

Both Allred and Kramer, taken individually, fail to disclose or suggest the method of Claim 1. Further, neither reference teaches or suggests the features that are missing from the other. Hence, even if it is assumed, for the sake of argument, it would have been obvious to combine the references, the combination of Allred and Kramer would still fail to disclose or suggest all the features of Claim 1. For example, the combination still would not disclose or suggest generating one or more additional instances of a logic level representation for a representative memory cell to derive an abstracted memory column or representing a column of memory cells as a single-memory cell column comprising a representative memory cell. Therefore, the rejection of Claim 1 under 35 USC §103 is traversed, and Applicants respectfully submit that Claim 1 is allowable over the cited references.

Each of Claims 2-13 contains all the features of Claim 1 discussed above and are patentable for the same reasons discussed above with respect to Claim 1. Further, each of Claims 2-13 feature limitations that individually render them patentable. Due to the fundamental differences already identified, a separate discussion of those limitations is not included at this time. For all the foregoing reasons, Applicants respectfully submit that Claims 2-13 are allowable over the cited references.

Claims 14-39 each recite similar features as those discussed above with respect to Claim 1. For example, Claims 14-26 are recited in a format allowable by 35 USC §112, paragraph 6 and correspond to method Claims 1-13 discussed above. Claims 27-39 are computer-readable medium claims that correspond to method Claims 1-13. Therefore, Applicants respectfully submit that Claims 14-39 are patentable for at least the same reasons discussed above as to Claims 1-13.

The Applicants believe that all issues raised in the Office Action have been addressed and that allowance of the pending claims is appropriate. Entry of the amendments herein and further examination on the merits are respectfully requested.

The Examiner is invited to telephone the undersigned at (408) 414-1080 to discuss any issue that may advance prosecution.

No fee is believed to be due specifically in connection with this Reply. To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. § 1.136. The Commissioner is authorized to charge any fee that may be due in connection with this Reply to our Deposit Account No. 50-1302.

Respectfully submitted,

HICKMAN PALERMO TRUONG & BECKER LLP

Dated: October 26, 2005

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

on October 26 2005 (Date) by Trudy Bigdon (Signature)